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(54) Data transmission system.

(57) A data transmission system that permits data with the top priority to be transmitted preceding the other data when collision occurs in a data transmission network with a plurality of terminals. Each terminal (A, B, C) monitors the bus for a predetermined period (T_p) after the bus line becomes empty but immediately before the terminal is ready for data transmission so that, on detecting a signal on the bus during this predetermined period (T_p), the terminal starts transmitting data synchronously with the detected signal. As a result, data with the top priority is always allowed to pass through the circuit preceding other data despite a clock pulse difference between the terminals.

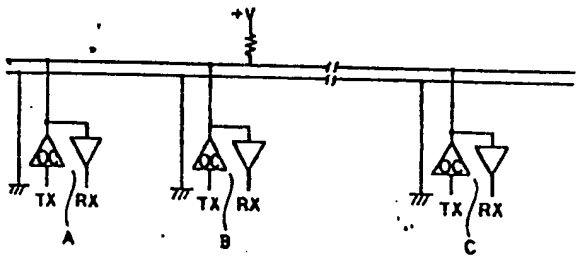

FIG.1

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DATA TRANSMISSION SYSTEM

The present invention relates to a data transmission system in a bus-type network such as used in home automation.

DESCRIPTION OF THE PRIOR ART

CSMA/CD has been proposed as a system for transmitting data via a bus-type network. With this system,a bus is monitored at all times so that a signal is transmitted promptly or after a predetermined period when no signal is detected on the bus. When data is output under the above condition, there is a possibility that data transmission is started simultaneously with that from another terminal due to a signal transmission delay.To avoid this data collision, the system is provided with means for detecting collision by comparing the output signal with a signal on the bus, so that data transmission is stopped when a collision is detected. In this case, the bus may be designed to permit either one of the colliding data to pass through the circuit.

Fig. 1 shows an example of this kind of bus with the simplest construction in which the bus is composed of wired OR circuits with open collectors. A, B and C are transmitting/receiving terminals.

Fig. 2 is a timing chart explaining the above-mentioned collision detection operation by the bus of Fig. 1. In this example, it is assumed that two terminals A and B start data transmission simultaneously at the point 0. After transmitting signals, the terminals A and B sample the signal on the bus. If the signal sampled by one of the terminals is different from that output by that terminal, the terminal stops data transmission immediately. Referring to Fig. 2, collision is not detected by any of the terminals at the sampling points T_1 and T_2 where the signal on the bus is identical with the one output by the two terminals A and B. At the pont T_3 where the signal on the bus is LOW though a HIGH level signal is output by the terminal B, the terminal B detects collision and stops the data transmission promptly. Meanwhile, the terminal A, which does not detect collision, continues data transmission. Thus, the data from the terminal A can pass through the circuit without being destroyed by the data from the terminal B.

Using the above system, it is possible to give higher priority to a particular data. Since a LOW signal is given higher priority than a HIGH level signal in this example, a

data with a series of LOW level signals for the leading bits is allowed to pass prior to other data, which is quite convenient in transmitting urgent data.

When the bus is busy, terminals which want to transmit data wait until the bus becomes unoccupied. The terminals may start data transmission all at once as soon as or in a predetermined period after the bus becomes empty. Collision probability is the highest at this time. Even if all the terminals start data transmission exactly at the same time, the data with the highest priority can be allowed to pass prior to other data in the above-mentioned system.

In actual operation with a simple CSMA/CD system, however, the data with the highest priority is not always allowed to pass prior to other data when the bus becomes empty. Fig. 3 is a timing chart showing the operational mode of this example in which the terminals A and B have different clock pulses. It is assumed that the clock for the terminal B is faster than that for the terminal A and that the data from the terminal A is given higher priority than that from the terminal B. Both terminals A and B start their respective timers at the point 0 where the bus becomes empty, so as to start data transmission after a predetermined period T_p. Actually, however, the terminal A starts data transmission at T_{pA}, reckoning that the predetermined period T_p has elapsed at T_{pA}, whereas the terminal B starts

data transmission at T_{PB}, reckoning that the predetermined period Tp has elapsed at T_{PB}. In this case, since the clock for the terminal B is faster than that for the terminal A, T_{PB} comes faster than T_{PA}. As a result, the terminal A cannot transmit data at T_{PA} because the bus line is occupied by data which the terminal B starts transmitting at T_{PB}. Thus, despite the higher priority of the data from the terminal A, the data from the terminal B is transmitted prior to the data from the terminal A; the terminal A is obliged to wait until the data from the terminal B has been transmitted.

As understood from the above, in data transmitting operation with the conventional simple CSMA/CD system, clock pulse error dominates the bit collation-based data priority immediately after the bus becomes unoccupied.

OBJECT AND SUMMARY OF THE INVENTION

OBJECT OF THE INVENTION

It is the object of the present invention to provide a data transmission system which, despite the clock pulse difference between terminals, can allow the data with the highest priority to pass through the circuit prior to other data,

in data transmission operation immediately after the bus becomes empty.

Other objects and further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. It should be understood, however, that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only; various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

SUMMARY OF THE INVENTION

According to the present invention, the bus line is monitored for a predetermined period so that, when a signal is detected on the bus line immediately before the terminal is ready for data transmission after the bus line becomes empty, the terminal starts data transmission in synchronization with the detected signal. As a result, the data with the highest priority is allowed to pass through the circuit prior to other data even if there is clock pulse difference between terminals.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be better understood from the detailed description given hereinbelow and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention and wherein:

Fig. 1 is a schematic chart showing a general bus structure;

Fig. 2 is a timing chart showing an operational mode of the conventional system;

Fig. 3 is another timing chart showing another operational mode of the conventional system;

Fig. 4 is a timing chart showing an operational mode of an embodiment of a data transmission system of the present invention;

Fig. 5 is another timing chart showing another operational mode of an embodiment of the data transmission system of the present invention; and

Fig. 6 is a flow chart of a data transmitting routine conducted by the data transmission system of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 4 is a timing chart showing an operational mode of the present invention. It is designed that the terminals A and B start data transmission at the time T_p after the bus line becomes empty. It is assumed that the data from the terminal A is given higher priority than that from the terminal B. The terminals A and B start their respective timers at the point 0 where the bus line becomes empty, and monitor the bus at least for the period between T_f and T_p. If a terminal detects a signal on the bus line during this monitoring period, it starts data transmission promplty in synchronization with the signal. If the terminal detects no signal during this period, it starts data transmission at the point T_p.

In Fig. 4, the clock for the terminal A is slower than that for the terminal B. The terminal B starts its timer at the point 0 where the bus line becomes empty, and monitors the bus for the period between T_{fB} and T_{pB}. Detecting no signal during this period, the terminal B starts data transmission at the point T_{pB}. Similarly, the terminal A monitors the bus for the period between T_{fA} and T_{pA}. When it detects the signal output from the terminal B, it starts data transmission synchronously with the signal. Since the data from the terminal A is given higher priority

than that from the terminal B, the terminal B detects collision at the point C and stops data transmission, so that only data from the terminal A survives. Thus, data from the terminal A with a slower clock can be transmitted prior to data from the terminal B with a faster clock.

Fig. 5 is a timing chart for the case where the clock of the terminal A is faster than that of the terminal B. Similar to the previous example, the terminal A monitors the bus for the period between T_{fA} and T_{pA}. Since it detects no signal during this period, it starts data transmission at the point T_{pA}. Meanwhile, the terminal B detects the signal output from the terminal A during the period between T_{fB} and T_{pB} and promptly starts data transmission. However, the terminal B detects collision at the point T_C and stops data transmission, so that no problem occurs.

Thus, according to the present invention, data with the higher priority from the terminal A always precedes data from the terminal B in data transmission operation under any condition. In any of these embodiments, it is necessary to set T_f smaller than T_p counted by the fastest clock in the system.

Fig. 6 is a flow chart showing a signal transmitting routine of the present invention. If there is no data detected on the bus through the period of T_p or longer, a terminal can transmit data at any time (The routine skips

form STEP 1 to STEP 6). If there is data on the bus, the terminal waits until the time T_f elapses after the bus becomes empty. If there is no data on the bus and if the time T_f has not elapsed, the terminal waits until the time T_f elapses (STEP 2 and STEP 3). If a terminal detects a signal on the bus during the period between T_f and T_p, it starts data transmission immediately (The routine skips from STEP 4 to STEP 6). If no signal is detected during this period, the terminal starts data transmission at the point T_p (The routine proceeds from STEP 5 to STEP 6). The above-mentioned data transmission is conducted by this processing routine.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications are intended to be included within the scope of the following claims.

C L A I M S

1. In a network comprising a data transmission system which permits data to be output onto a bus at any desired time when no data has been detected on the bus for a continuous predetermined period or longer immediately before the data transmission and which allows data with the top priority to pass through the circuit preceding the other data even when a plurality of terminals output data all at once, the data transmission system being c h a r a c t e r i z e d in that a terminal with intention of transmitting data waits for a predetermined no-data period T_f, which is shorter than the time period T_p elapsed since the bus became empty and starts data transmission in synchronization with a signal if detected during the monitoring period between T_f and T_p, or starts data transmission at the time T_p if data is not detected during said monitoring period.

2. The data transmission system of claim 1, wherein said predeterminde period T_f is set shorter than the fastest T_p count of the plurality of terminals.

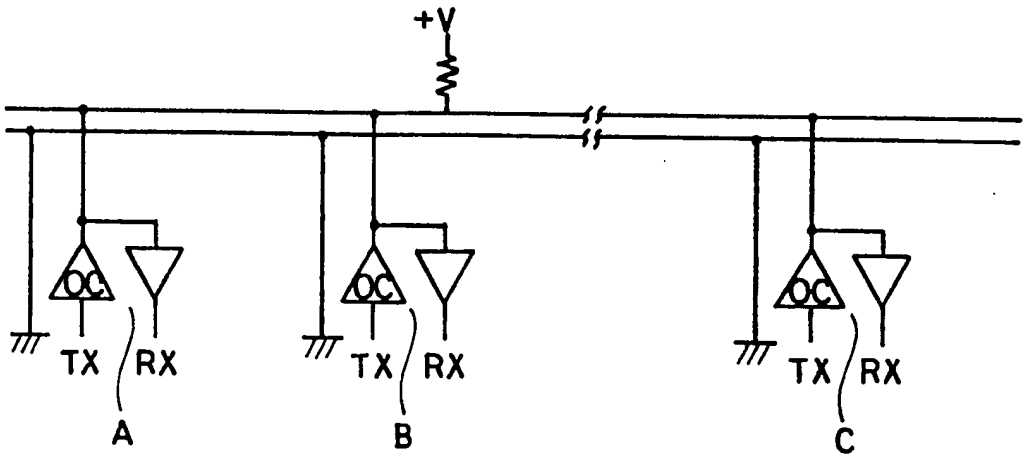

FIG.1

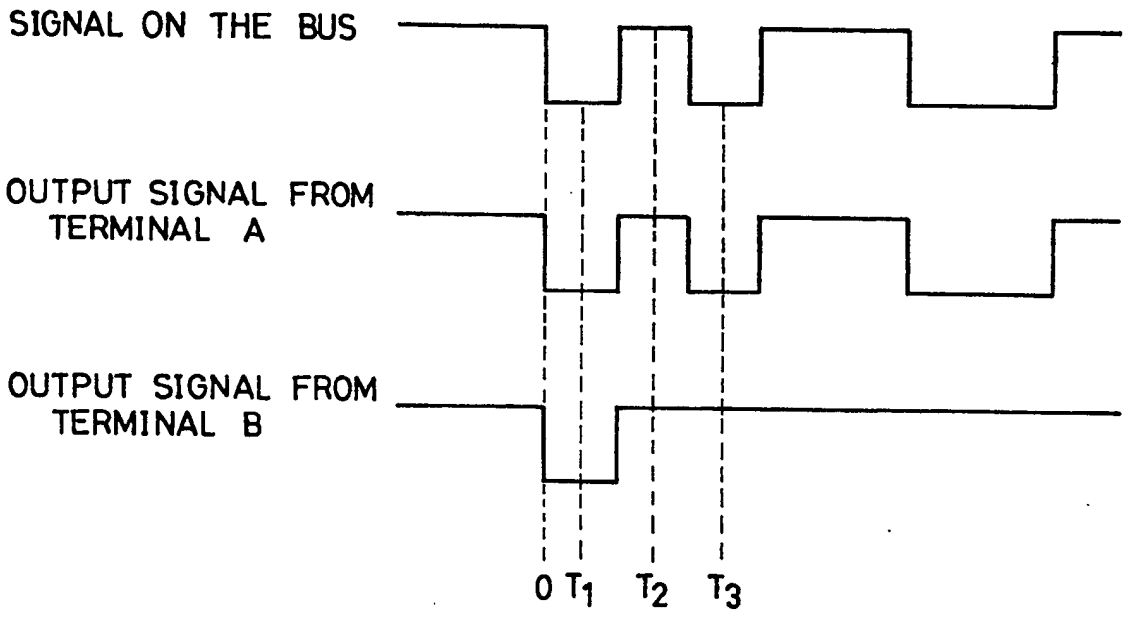

FIG.2 PRIOR ART

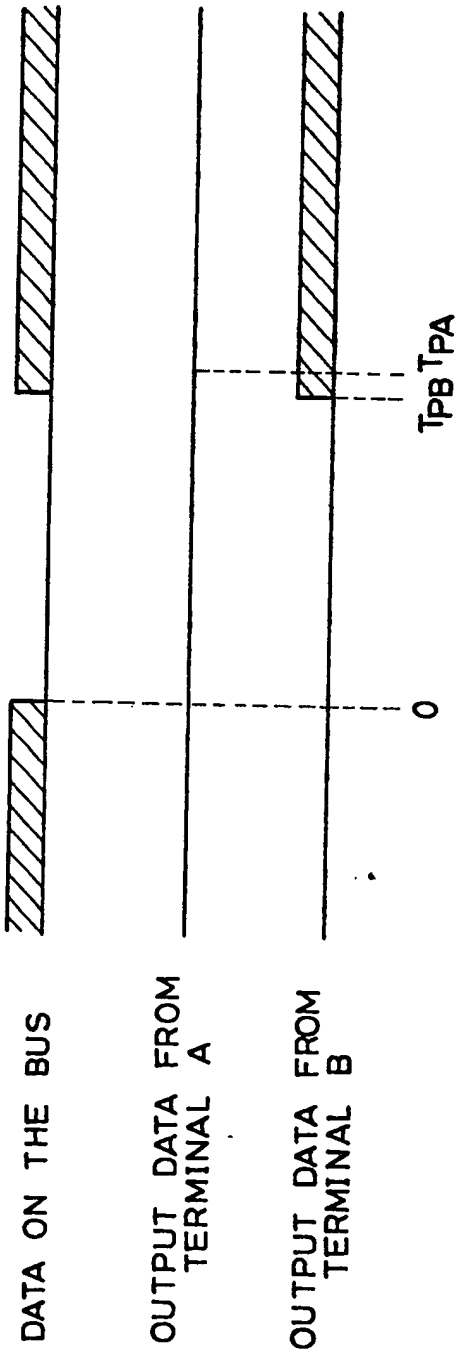
DATA ON THE BUS
OUTPUT DATA FROM TERMINAL A
OUTPUT DATA FROM TERMINAL B
0
TPB TPA

FIG.3

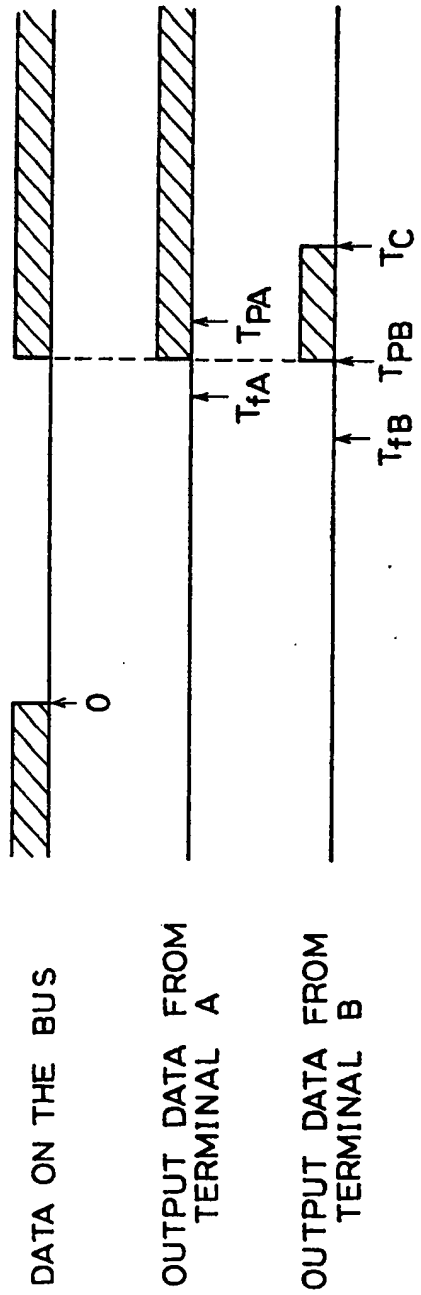
DATA ON THE BUS
OUTPUT DATA FROM TERMINAL A
OUTPUT DATA FROM TERMINAL B
0
T_{PA}
T_{fA}
T_{PB}
T_C
T_{fB}

FIG. 4

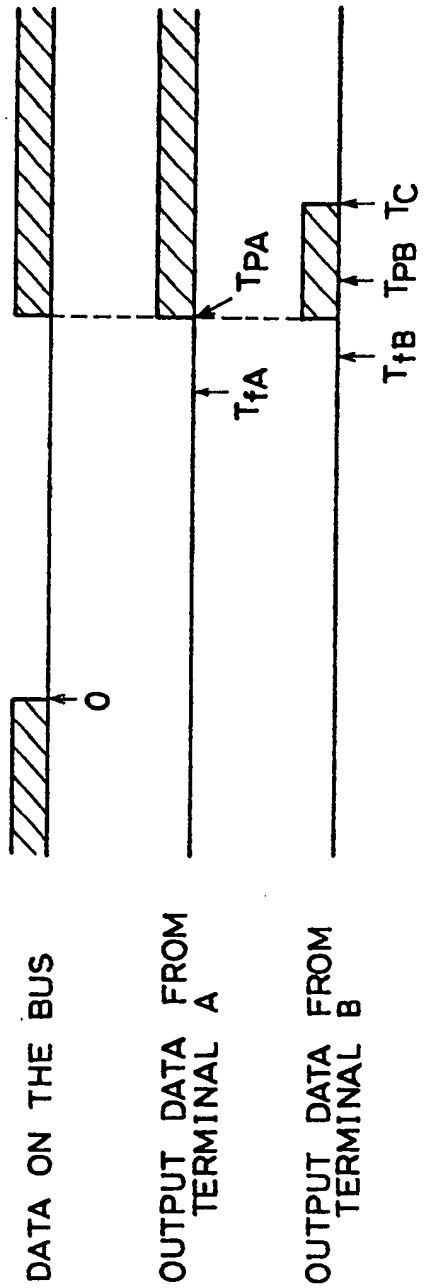
DATA ON THE BUS
OUTPUT DATA FROM TERMINAL A
OUTPUT DATA FROM TERMINAL B
0
T_{PA}
T_{fA}
T_{PB}
T_C
T_{fB}

FIG. 5

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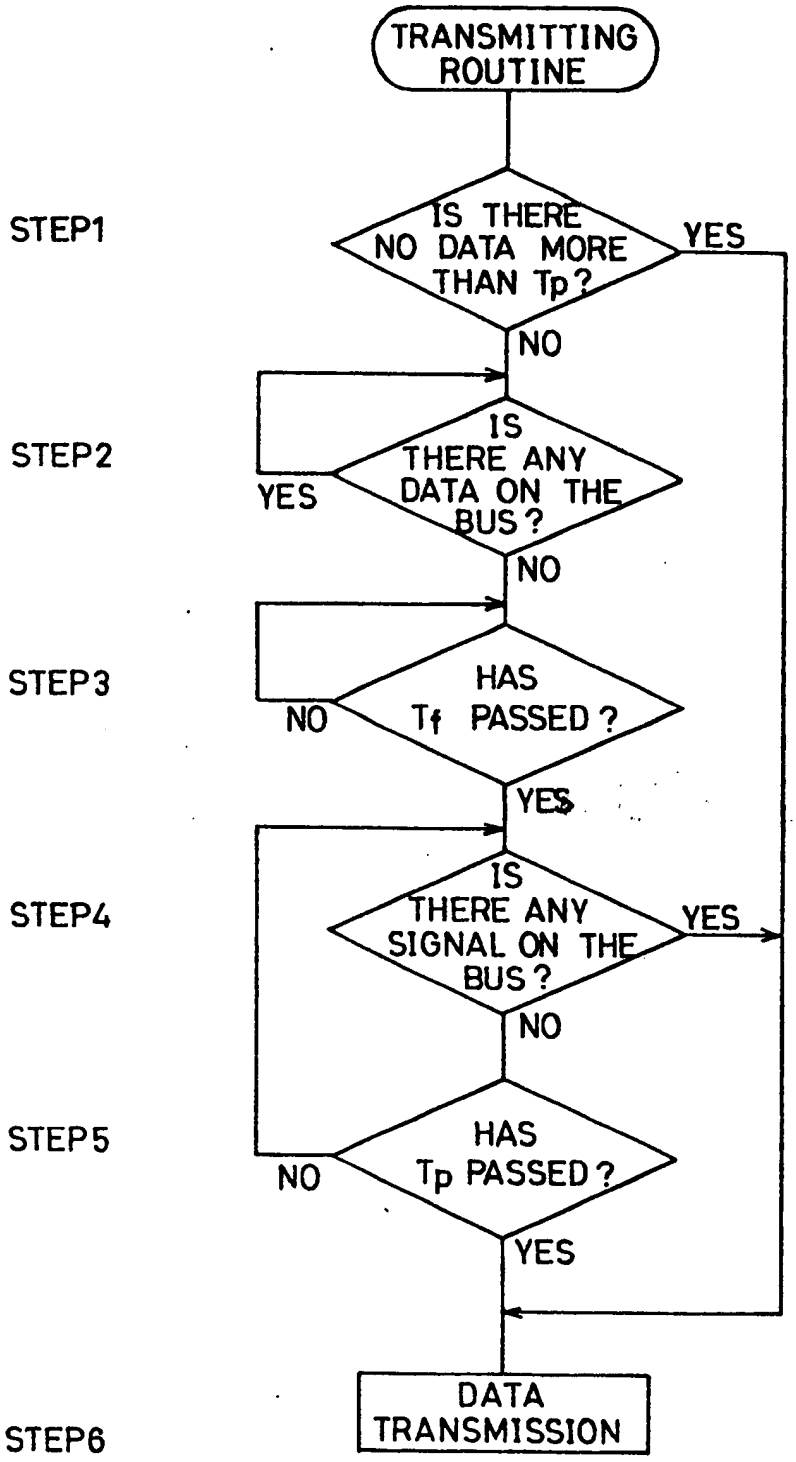

FIG.6